IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application. An identifier indicating the status of each claim is provided.

Listing of Claims

1. (Currently Amended) A polyphase filter having N branch allpass filters of order x · N that filter an input signal, said polyphase filter comprising:

a structure of an allpass filter of order x comprising delay elements with a ~~delay of 1~~ delay of N and at least one multiplier, ~~wherein all the delay elements with the delay of 1 are replaced by~~ wherein delay elements with a delay of N ~~in order to~~ decrease a sampling rate of each of the N branch allpass filters of order x · N,

wherein the sampling rate $fS' = fs/N$, with fs being the sampling rate of the input signal, for each of the N branch allpass filters of order x · N, where x is an integer number and N is a decimation factor of the polyphase filter; and

wherein said polyphase filter increases a number of Intermediate Frequencies (IF) utilized in selecting the sampling ~~frequency~~ rate.

2. (Previously Presented) The filter according to claim 1, wherein each of said at least one multiplier comprises N time-multiplexed multiplication coefficients that are used in a predetermined order.

3. (Currently Amended) The filter according to claim 1, further comprising:

a first delay element with the delay of N that receives the input signal;

a first adder that receives an output signal of said first delay element at a first input for a first summand;

a second delay element with the delay of N that receives a sum produced by said first adder;

a first subtracter that receives the input signal at ~~a~~ the first input for a minuend and the output signal of the second delay element at a second input for a subtrahend; and

a first multiplier that receives a calculated difference of the first subtracter, multiplies ~~said first subtracter~~ said calculated difference of first subtracter with a predetermined multiplication coefficient and outputs a calculated product to the second input of the first adder that receives a second summand, wherein

~~in case~~ if x equals to 1, the sum produced by said first adder ~~builds~~ is accumulated to build the output signal ~~out of~~ from the branch allpass filters.

4. (Currently Amended) The filter according to claim 3, further comprising:

a second adder that receives the output signal of the second delay element at the first input for the first summand;

a third delay element with the delay of N that receives the sum produced by said second adder;

a second subtracter that receives the sum produced by said first adder at the first input for the minuend and the output signal of the third delay element at the second input for the subtrahend; and

a second multiplier that receives the calculated difference of the second subtracter, multiplies ~~said second subtracter~~ said calculated difference of the second subtracter

with a predetermined multiplication coefficient and outputs the calculated product to the second input of the second adder that receives the second summand, wherein

~~in case~~ if x equals to 2, the sum produced by said second adder is accumulated to build ~~builds~~ the output signal ~~out of~~ from the branch allpass filters.

5. (Previously Presented) The filter according to claim 2, wherein each of said at least one multiplier has quantized coefficients so that each of said at least one multiplier is realized by at least one shift register, at least one adder or at least one subtracter.

6. (Currently Amended) The filter according to claim 5, wherein each of said at least one multiplier comprises:

a first shift register that has a shift value of 2 and that receives a multiplicand and,

an input selector switch that receives an output value of said first shift register at a first fixed input terminal and the multiplicand at a second fixed input terminal,

a second shift register, a third shift register and a fourth shift register, an input of each of the second, third and fourth shift registers being connected to a moveable output terminal of said input selector switch.

a third subtracter that receives the output value of said second shift register at ~~a~~ the first fixed input terminal receiving a minuend,

a first output selector switch having a moveable input terminal connected to an output of said third shift register and the second fixed output terminal is connected to a second input of the third subtracter that receives a subtrahend,

a third adder that receives the output value of said third subtracter and that receives a first summand, and outputs the multiplied multiplicand,

a second output selector switch having a moveable input terminal connected to an output of said fourth shift register and the second fixed output terminal is connected to a second input of the third adder that receives a second summand.

7. (Currently Amended) The filter according to claim 1, wherein the polyphase filter of order $x \cdot N$ with $x = a$ is ~~realized~~ utilized in a time multiplex and ~~works with~~ uses a clock frequency $fc = a \cdot fs$, where x and a are integer numbers.

8. (Currently Amended) An IQ-generator comprising:

a multiplier for multiplying an incoming sampled bandpass signal by a signal ~~A(k)=(-1)floor (k/N)~~ $A(k)=(-1)^{\text{floor }(k/N)}$ and outputting a signal t(k); and

a polyphase filter having N branch allpass filters of order $x \cdot N$, having an input coupled to the output of said multiplier, and having a sampling frequency, where k is an input value, N is a decimation factor of the polyphase filter, x is an integer number, A(k) is a first signal and floor(x) is the greatest integer function, which gives the largest integer less than or equal to x; and

wherein said polyphase filter increases a number of Intermediate Frequencies (IF) utilized in selecting the sampling frequency.

9. (Currently Amended) ~~An~~ The IQ-generator according to claim 8, wherein the output signal of the polyphase filter having N branch allpass filters is multiplied by a signal $B(k) \cdot \cos(2\pi fo/fs \cdot k)$ to calculate an I-component of a complex baseband signal and by a signal

$B(k) \cdot \sin(2\pi fo/fs \cdot k)$ to calculate a Q-component of the complex baseband signal with ~~$A(k)=B(k)=(-1)^{floor(k/n)}$~~ $A(k)=B(k)=(-1)^{floor\,(k/N)}$, where fs is the sampling frequency, fo is a center frequency of the input signal, n is an integer number in the range of [-N/2...N/2] and B(k) is a second signal.

10. (Currently Amended) ~~An~~ The IQ-generator according to claim 8, wherein the incoming sampled bandpass signal is multiplied by the signal ~~$A(k)=(-1)^{floor\,(k/N)}$~~ $A(k)=(-1)^{floor\,(k/N)}$ before being supplied as the input signal to the polyphase filter consisting of N branch allpass filters of order $x \cdot N$, wherein the polyphase filter filters an I-component and a Q-component of a complex baseband signal.